Synthesis of Si nanowires at Low Temperatures

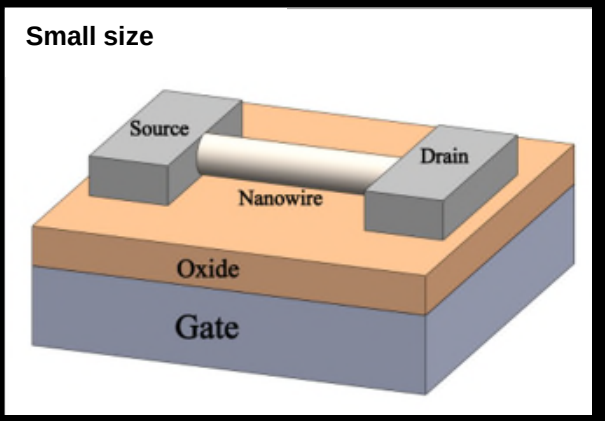
Luyao Ma
Advisor: Professor Stephen Maldonado
2015 Michigan Green Chemistry and Engineering Conference
University of Michigan

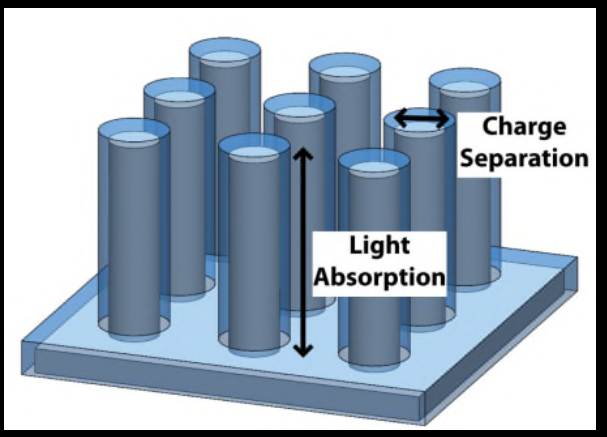
Why Si ?

- Semiconducting property
- 2nd most abundant element in the earth's crust

Why nanostructured Si (Si nanowire) ?

- Semiconducting property
- 2nd most abundant element in the earth's crust





Kelzenberg M. D.; *et al.*, *Nat. Mat.*, **2010**, *9,* 239.
Fan Z.; *et al.*, *PNAS.*, **2008**, *105,* 11066.

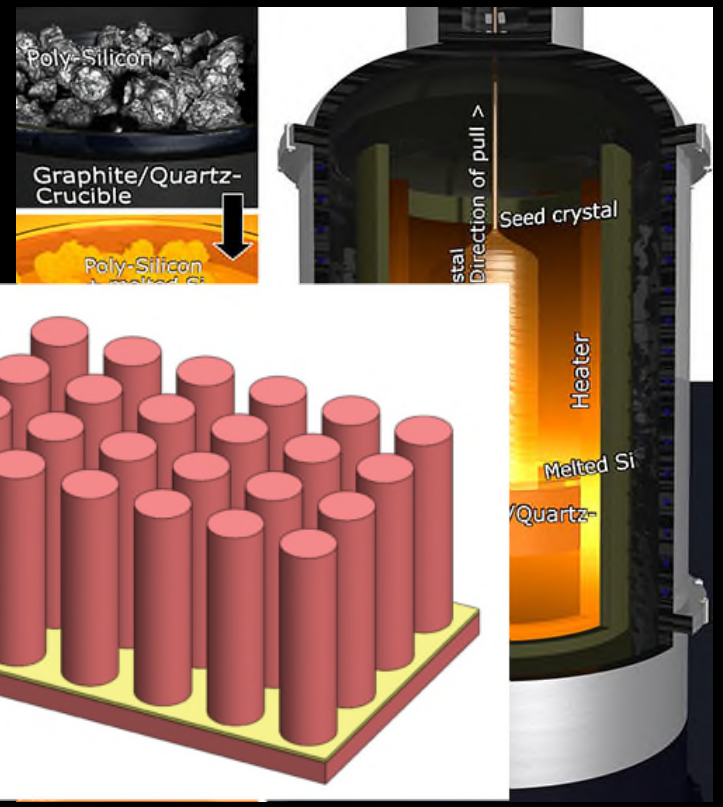
Is nano Si affordable?

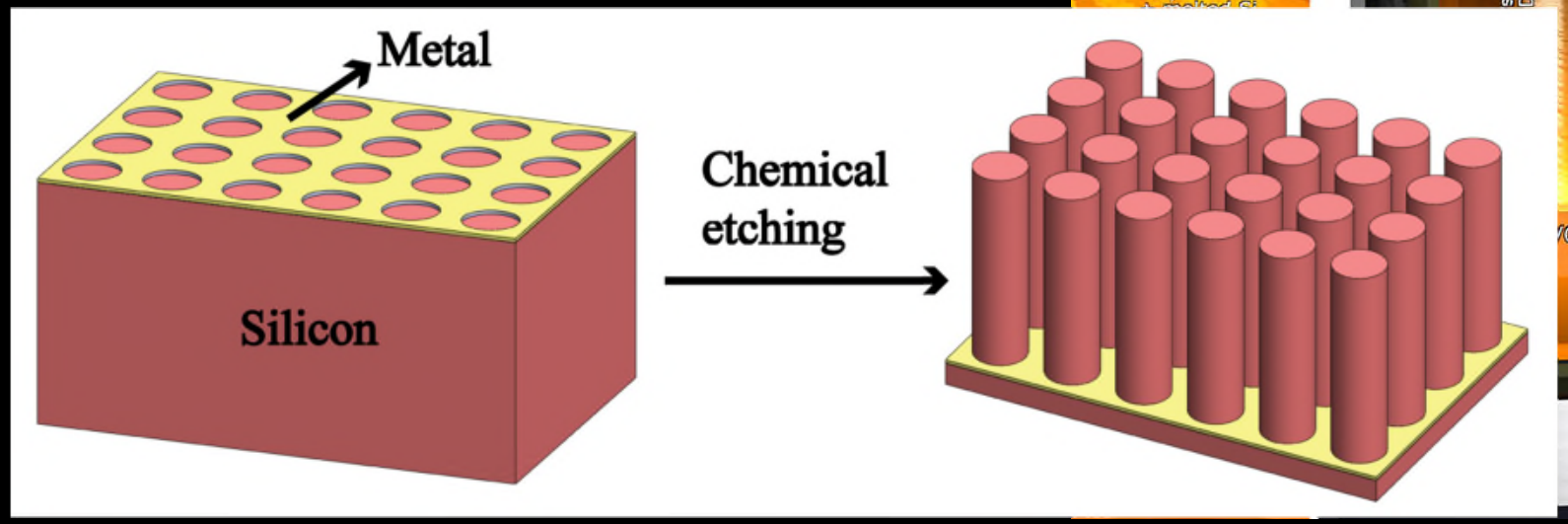
Yes.

But it’s not ‘green’

Nanostructured Si (Si nanowire) Preparation Methods

- Top-down
  - Czochralski process (> 1000 °C)
    - Energy intensive
  - Chemical etching
    - Waste of material



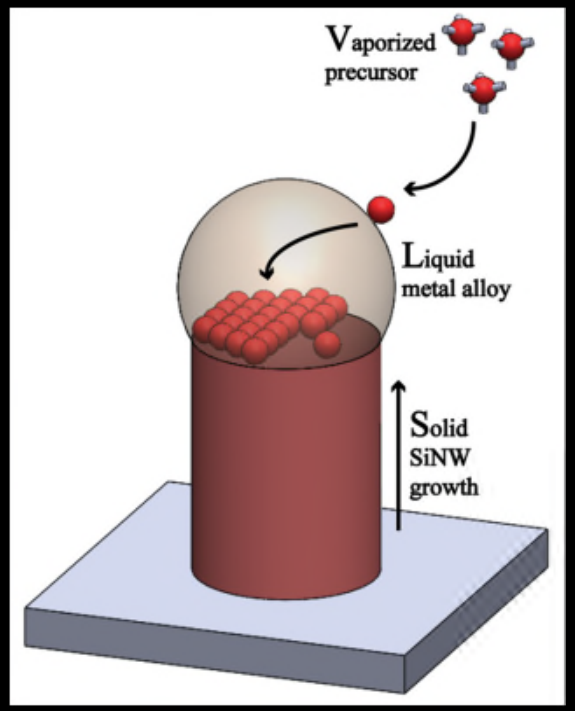


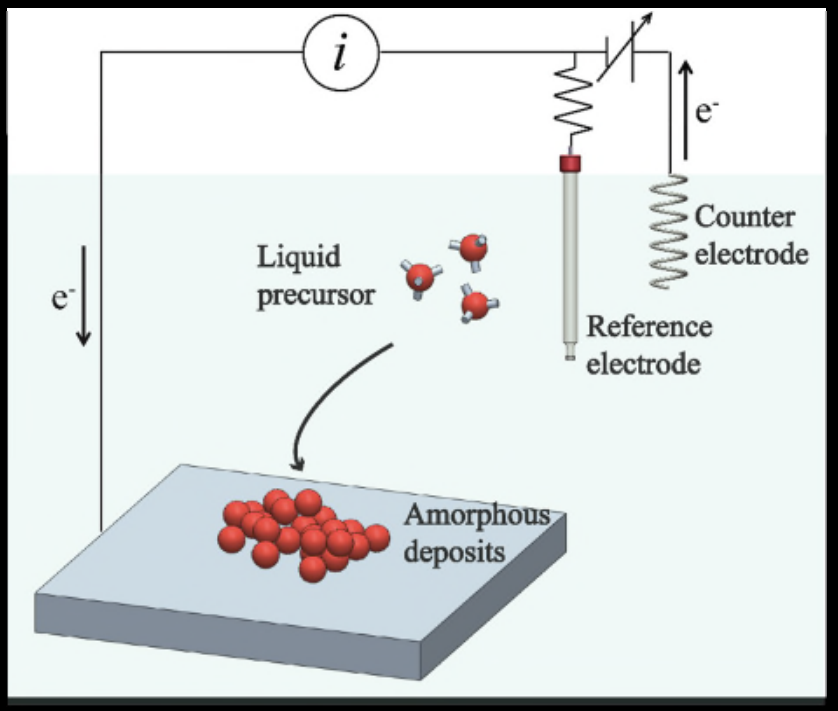
- Bottom-up
  - Vapor-liquid-solid (VLS) mechanism

Hsu C.M.; *et al., Appl. Phys. Lett.* **2008** , *93* , 133109
Chern W.; *Nano Lett.* **2010,** *10*, 1582–1588
http://www.microchemicals.com/products/wafers/silicon_ingot_production.html

Si nanowire Preparation Methods

- Bottom-up
  - Vapor-liquid-solid (VLS) mechanism
  - Low-temperature electrodeposition



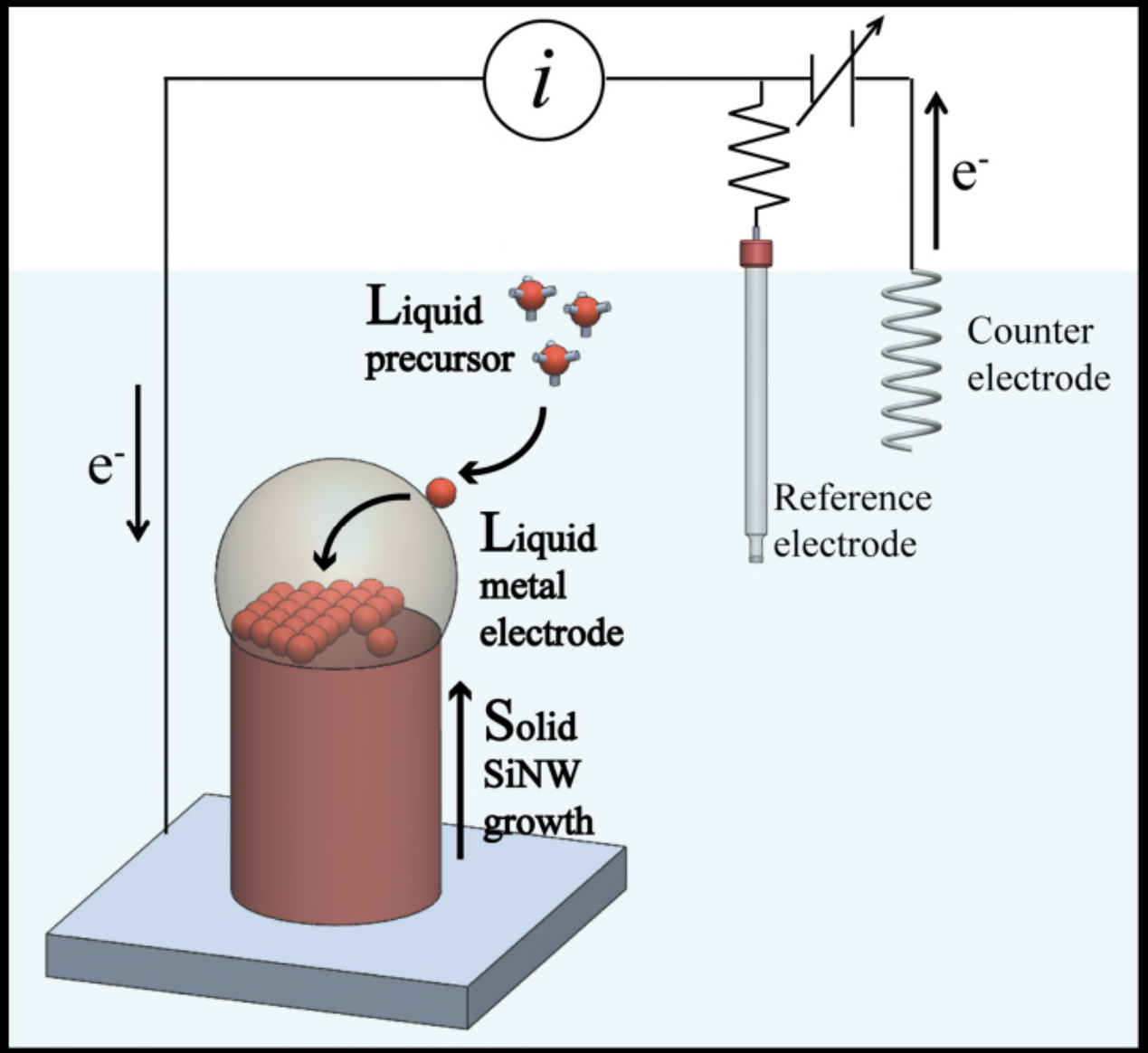


a) Chemical vapor deposition (CVD)
b) Molecular Beam Epitaxy (MBE)
c) Laser Ablation
   - Energy-intensive conditions
   - Costly instrumentation

a) Aprotic organic solvent
b) Ionic liquid
   - Amorphous deposits at low temperatures

Wagner, R. S.; Ellis, W. C. *Appl. Phys. Lett.* **1964**, *4*, 89.
V. Schmidt, *et al.*; *Chem. Rev.* **2010**, *110*, 361

Electrochemical liquid-liquid-solid process
- electrochemical analog of VLS



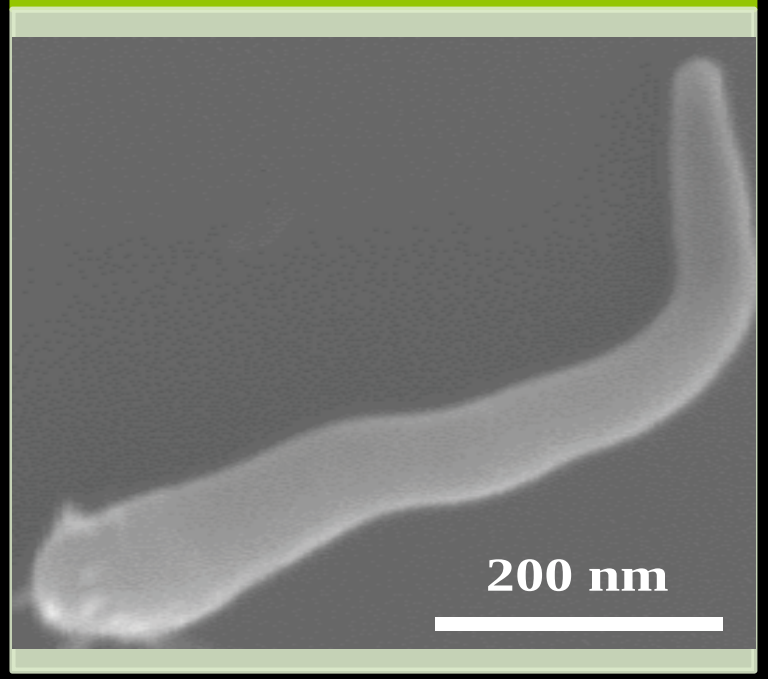
Ec-LLS

- **Low melting point liquid metal (e.g. Ga (l), Ga/In (l)) nanodroplet**
  - ➢ Working electrode
  - ➢ Mediate phase for crystallization

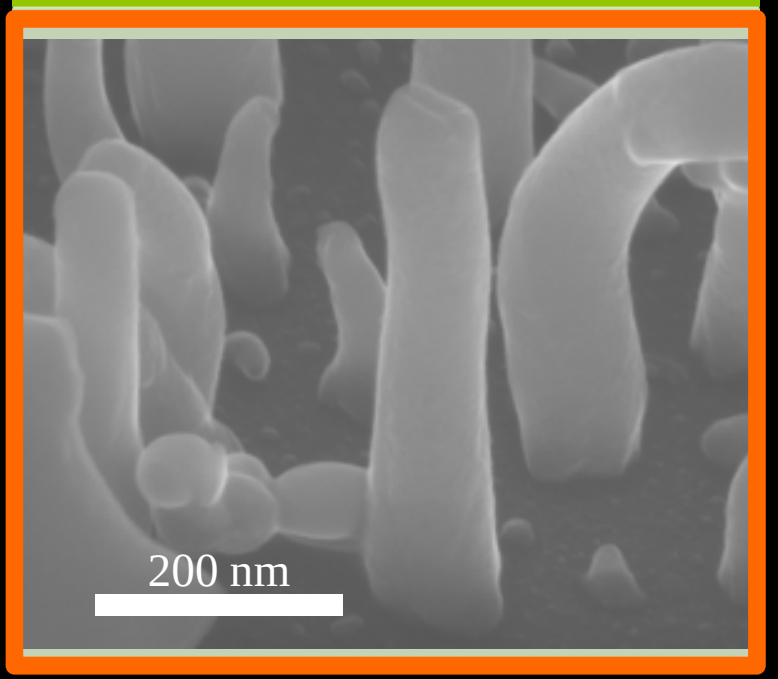
✓ Crystalline Si
✓ Low temperature process
✓ Simple setup

Group IV semiconductor nanowires prepared through ec-LLS process

Ge nanowires



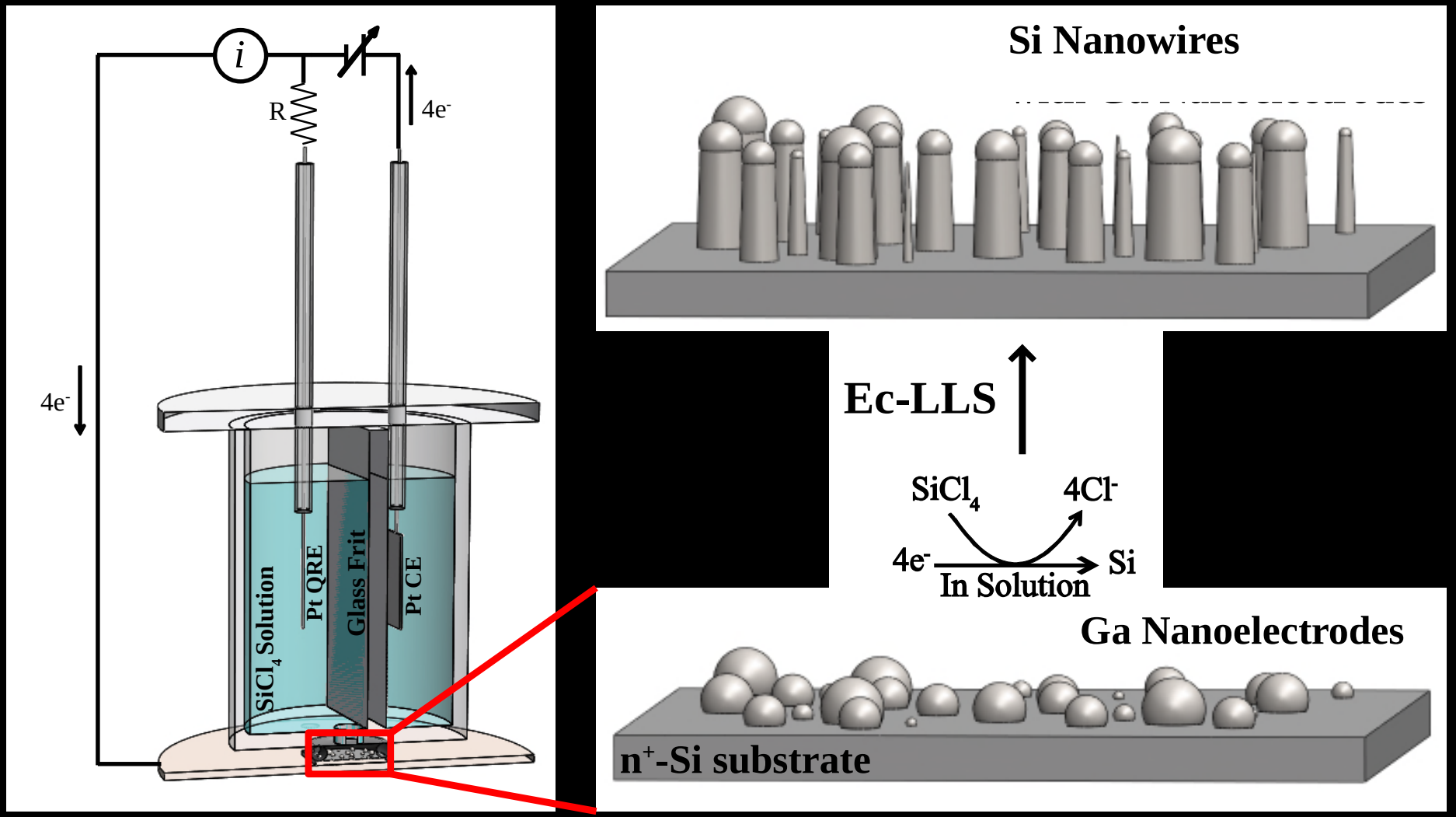
Si nanowires



Carim, A. I.; *et al*, *J. Am. Chem. Soc.* **2011**, *133*, 13292.
Gu, J., *et al*, *J. Am. Chem. Soc.*, **2013**, *135* (5), pp 1684.
Ma, L.; *et al*, *J. Electrochem. Soc.*, **2014**, *161*, 7, D3044-D3050.
Fahrenkrug, E.; Gu, J.; *et al*, *Nano Lett.* **2014**, *14*, 847.
Ma, L,; et al, submitted.

Si nanowire ec-LLS

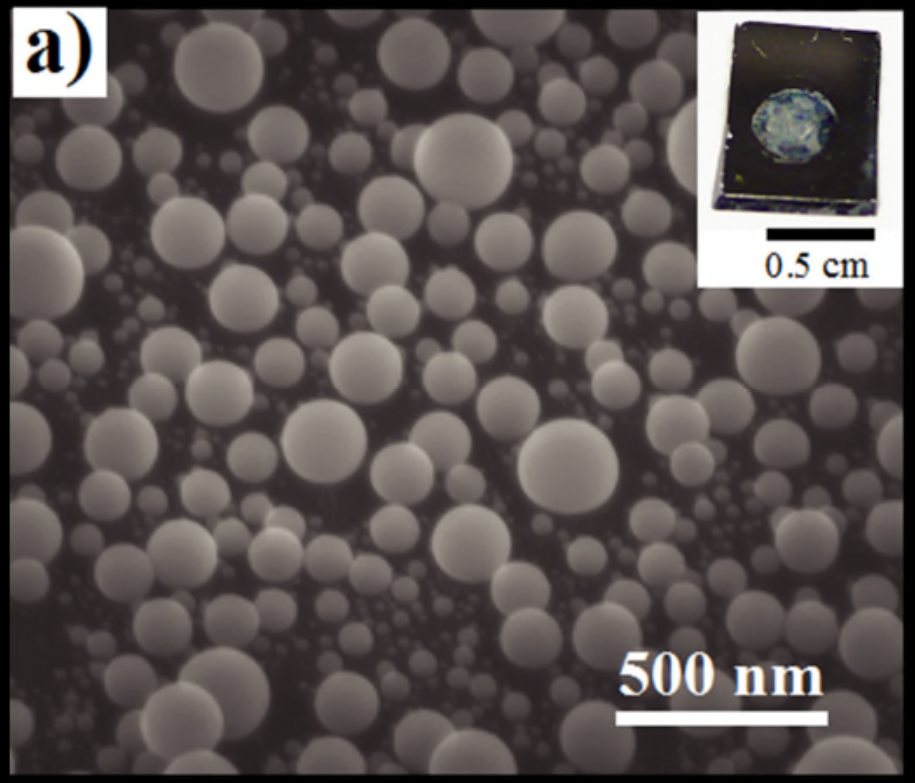
- Scheme

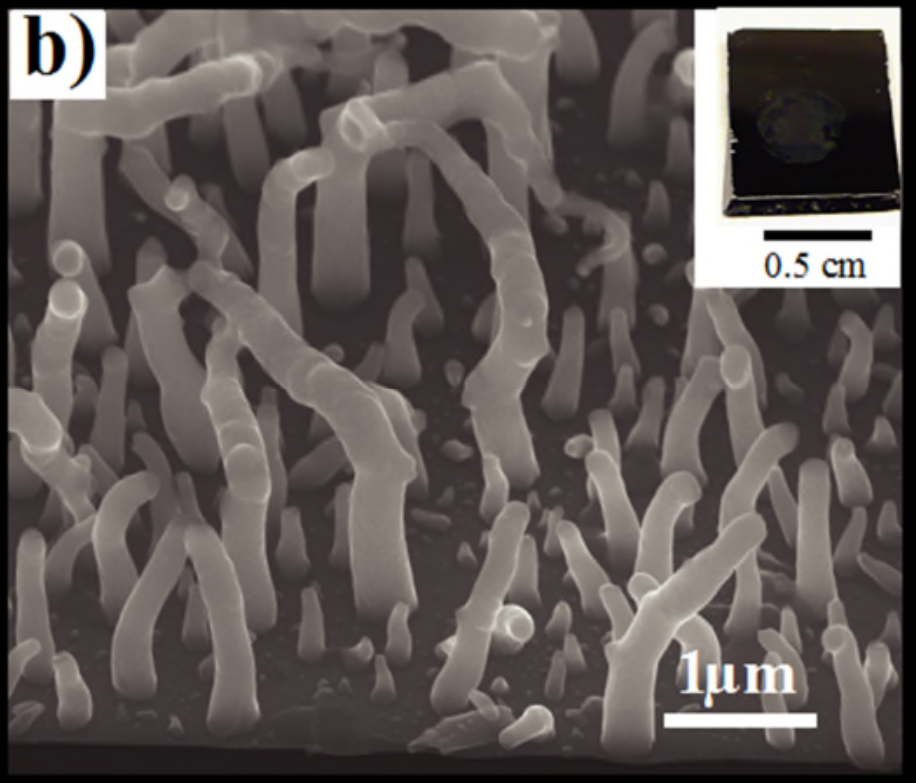


Scanning electron micrographs Si nanowires prepared at 120 °C through ec-LLS

Ga nanoparticles

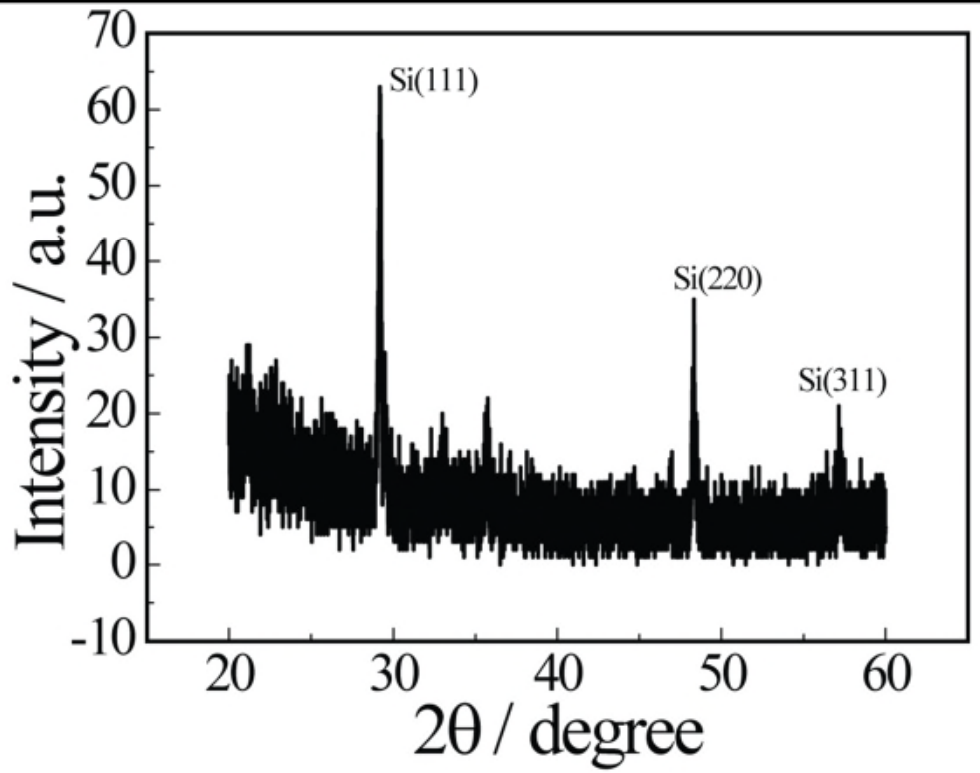
Si nanowires prepared after 40 mins' electrodeposition

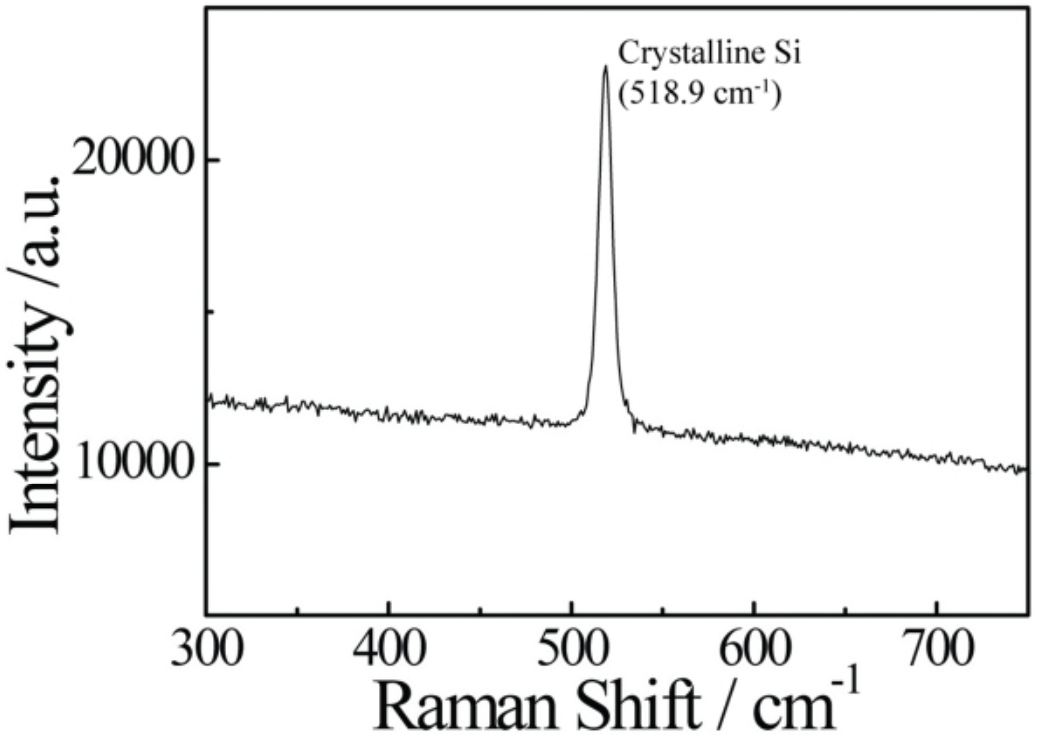




Characterization of SiNWs by X-ray diffraction & Raman spectroscopy

- X-ray diffractogram
- Raman spectrum



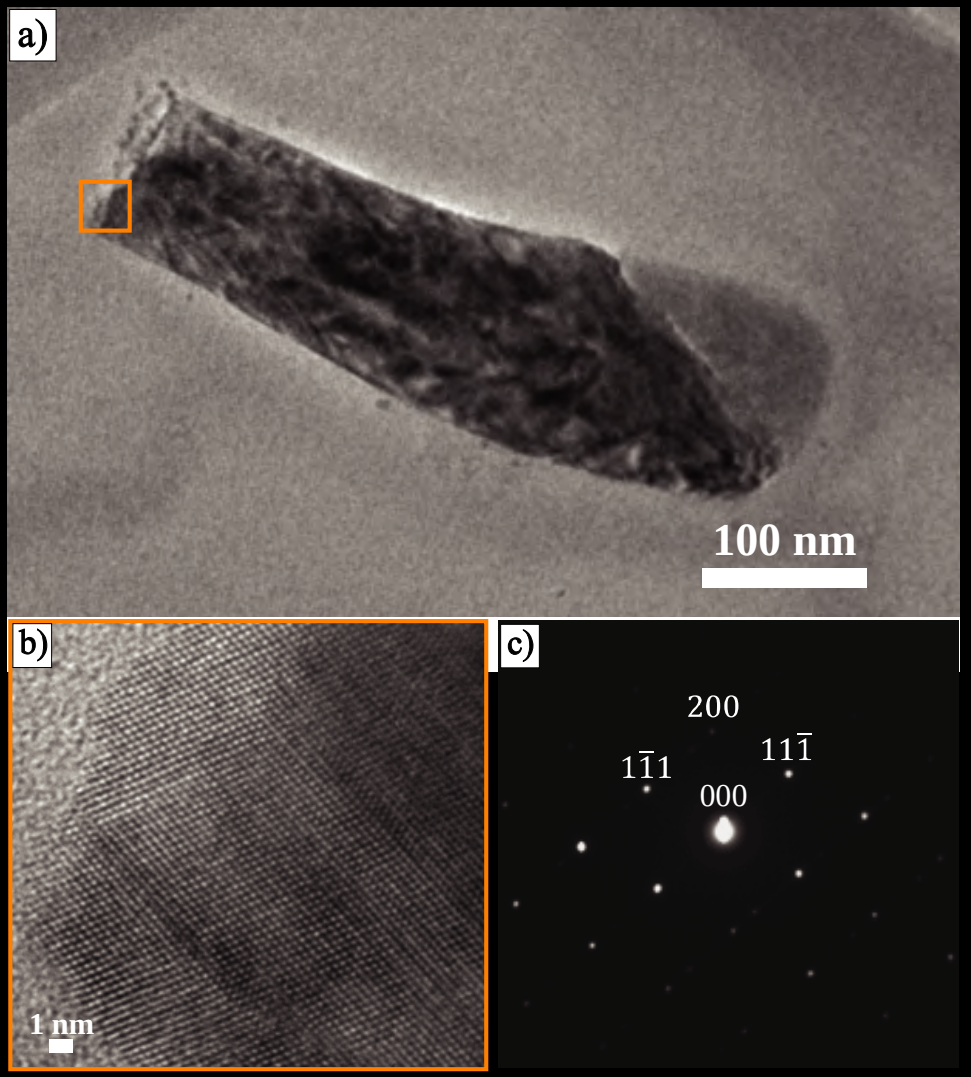


- **The Si nanowires are crystalline as examined by XRD and Raman**

H. Richter, Z.P. Wang & L. Ley, *Solid State Commun.* **1981**, *39*, **625.**

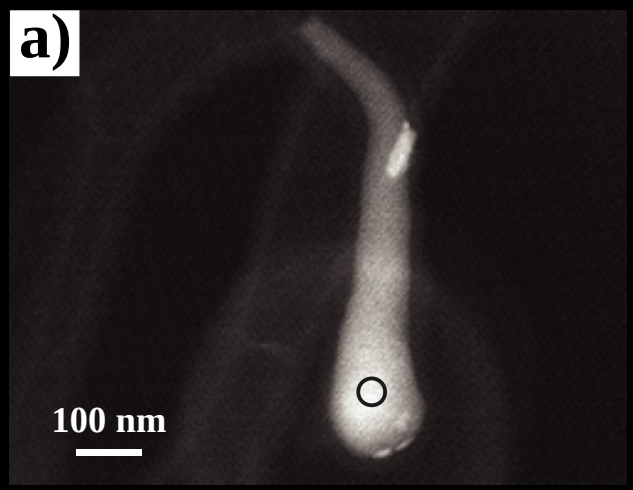
Crystallinity of a single Si nanowires shown by transmission electron microscope (TEM)

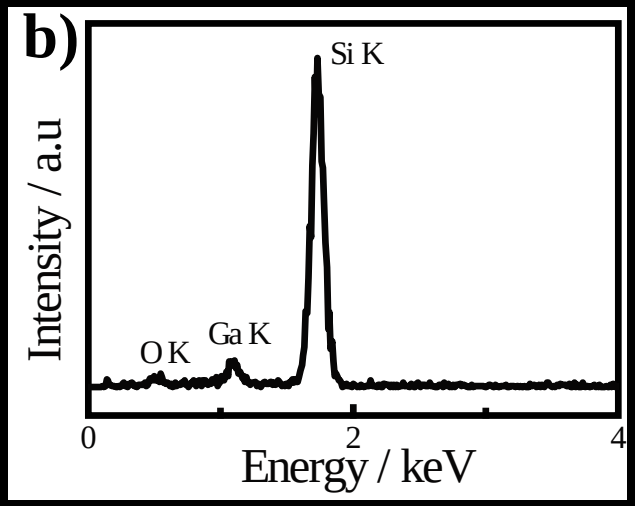
- Transmission electron micrograph of a single Si nanowire
- Mostly crystalline
- With defects

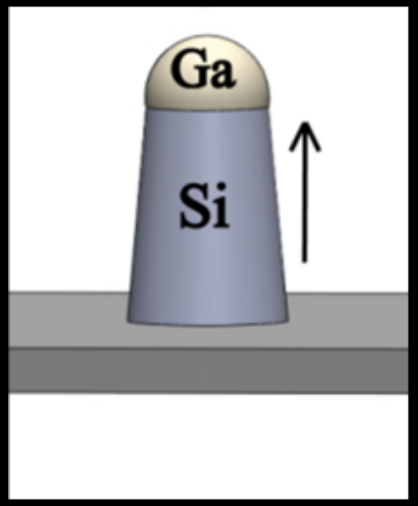


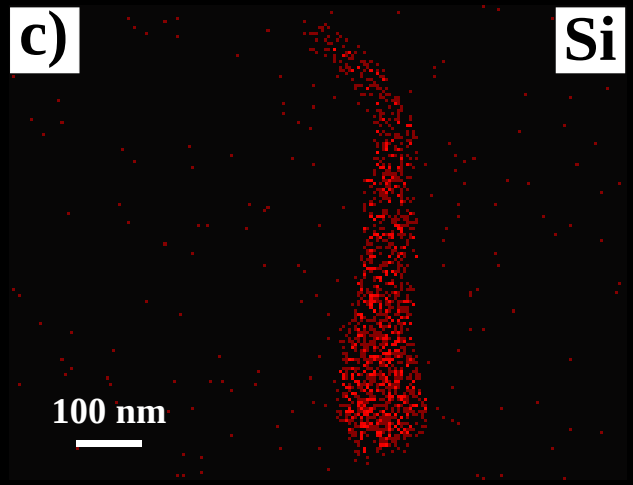
Chemical composition of a single nanowire examined by energy dispersive X-ray spectroscopy (EDS)

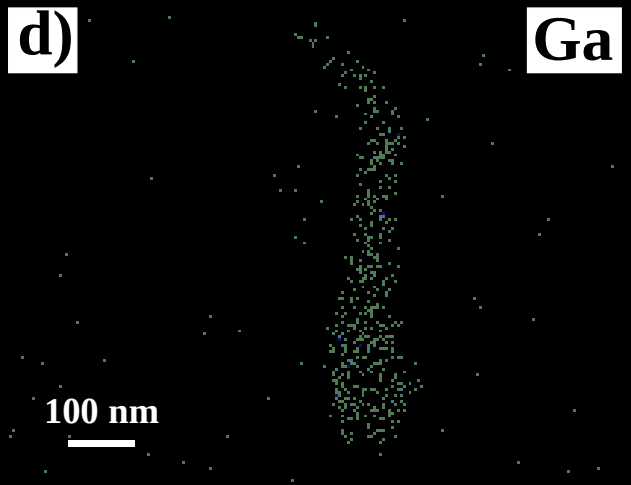
- Electron micrograph and X-ray spectrum were obtained under scanning TEM mode







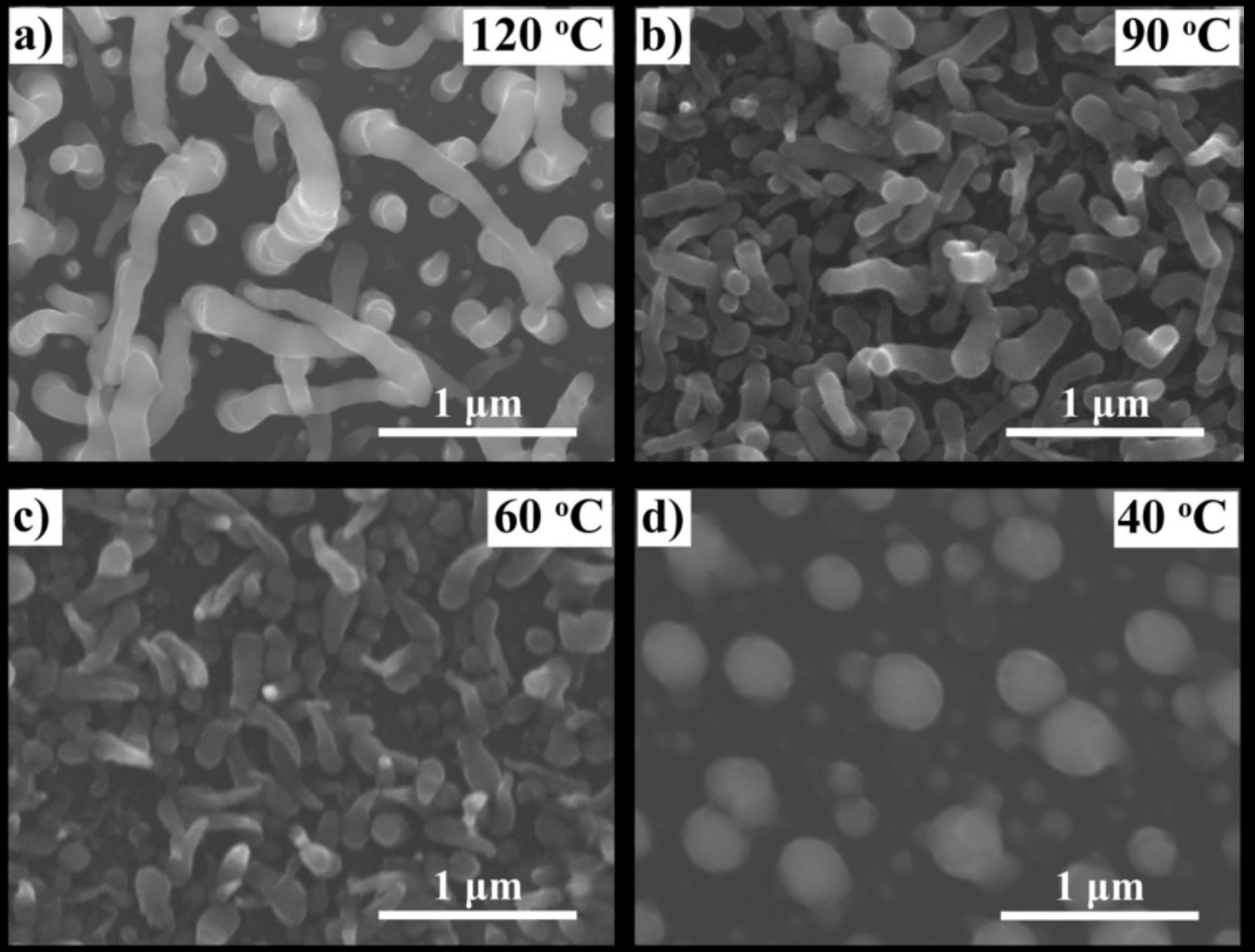




Ga incorporation into Si crystal causes the tapering of the nanowires

Exploring the effect of temperature on Ga incorporation

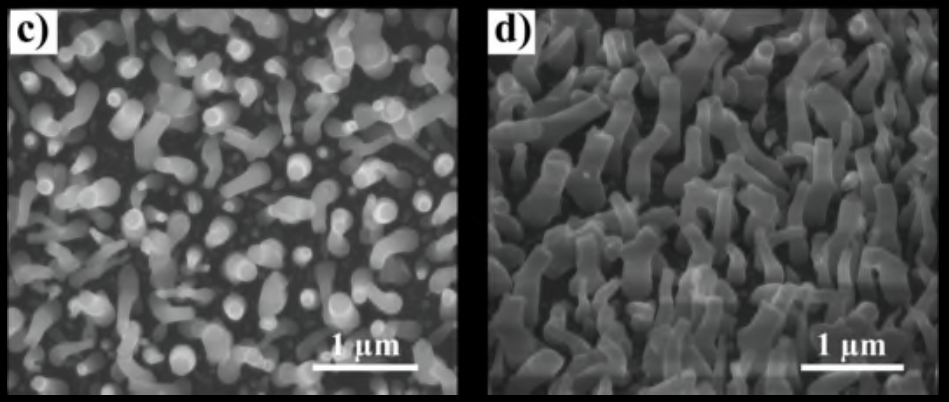
Temperature dependence of Si nanowire growth



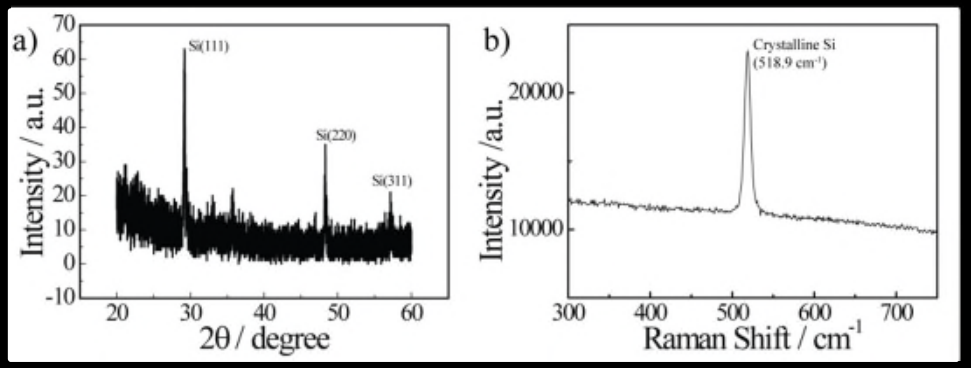
- **Temperature has no obvious effect on tapering**
- **Higher aspect ratio wires are prepared at 120 °C**
- **No Si nanowire growth observed at below 60 °C**

Summary

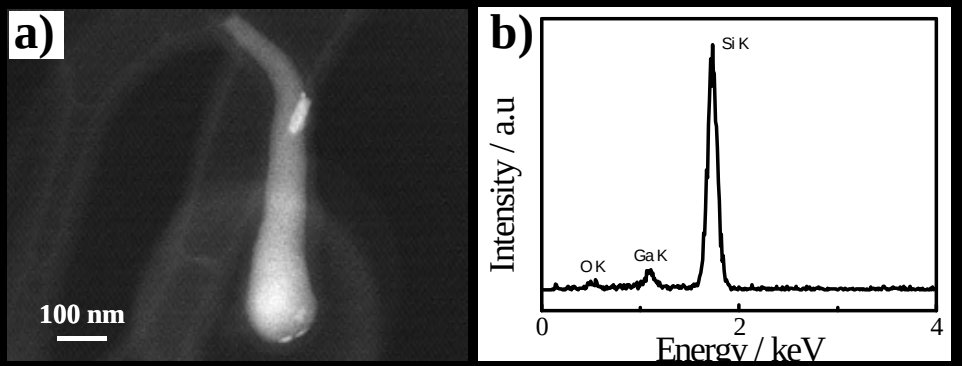
- Si nanowires are prepared via ec-LLS at below 100 °C



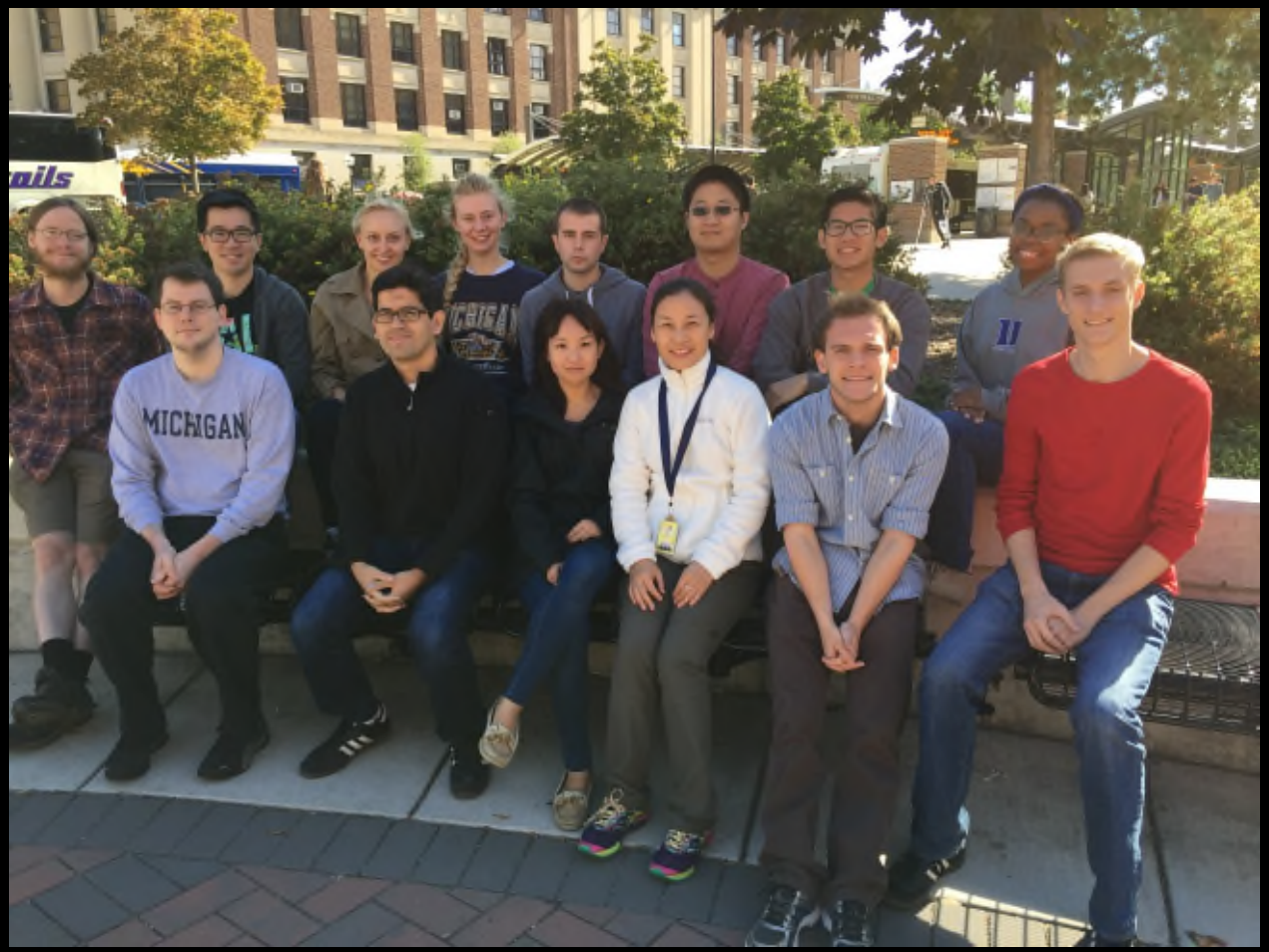
- As-prepared SiNWs are crystalline



- Ga incorporation results in tapering morphology

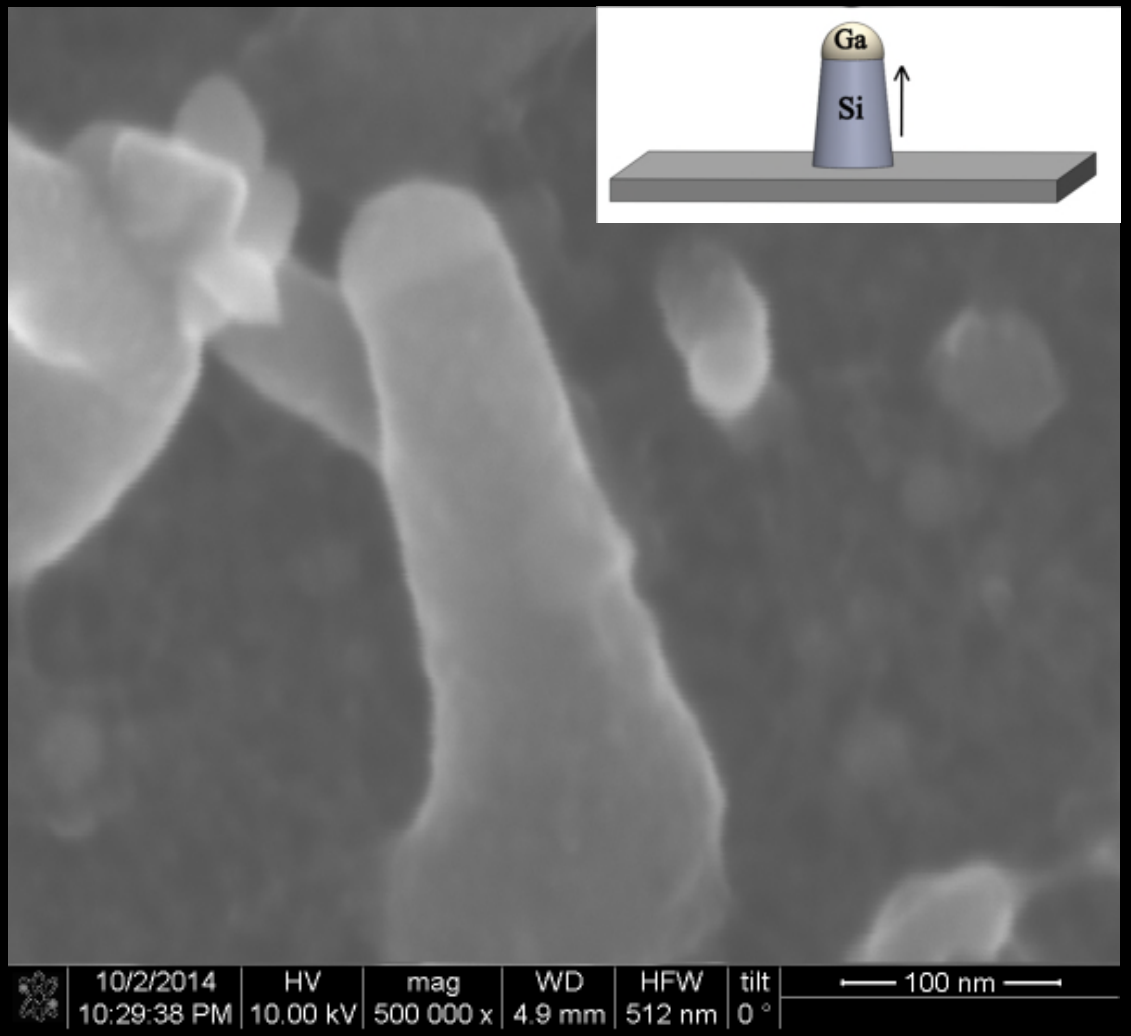


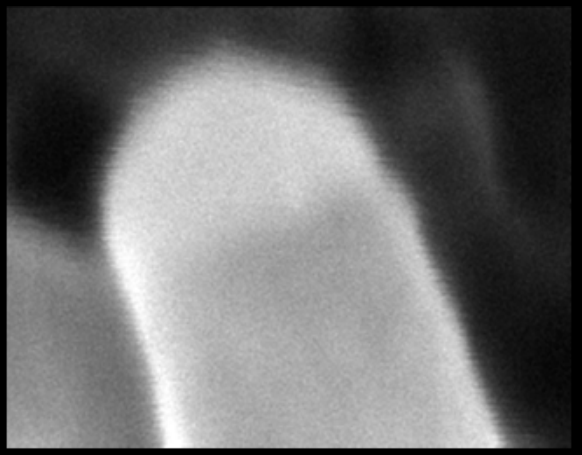
Acknowledgement

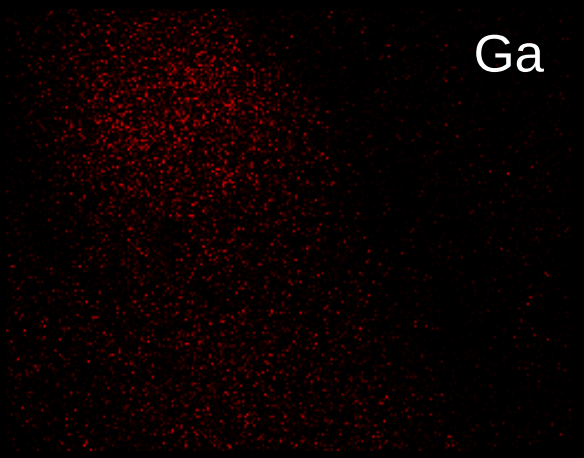


Prof. Maldonado
Susu for the help with TEM
Eli Fahrenkrug, Steve Donajkowski and Roy Wentz for the help with cell design
Maldonado Group

Ga during the crystal growth

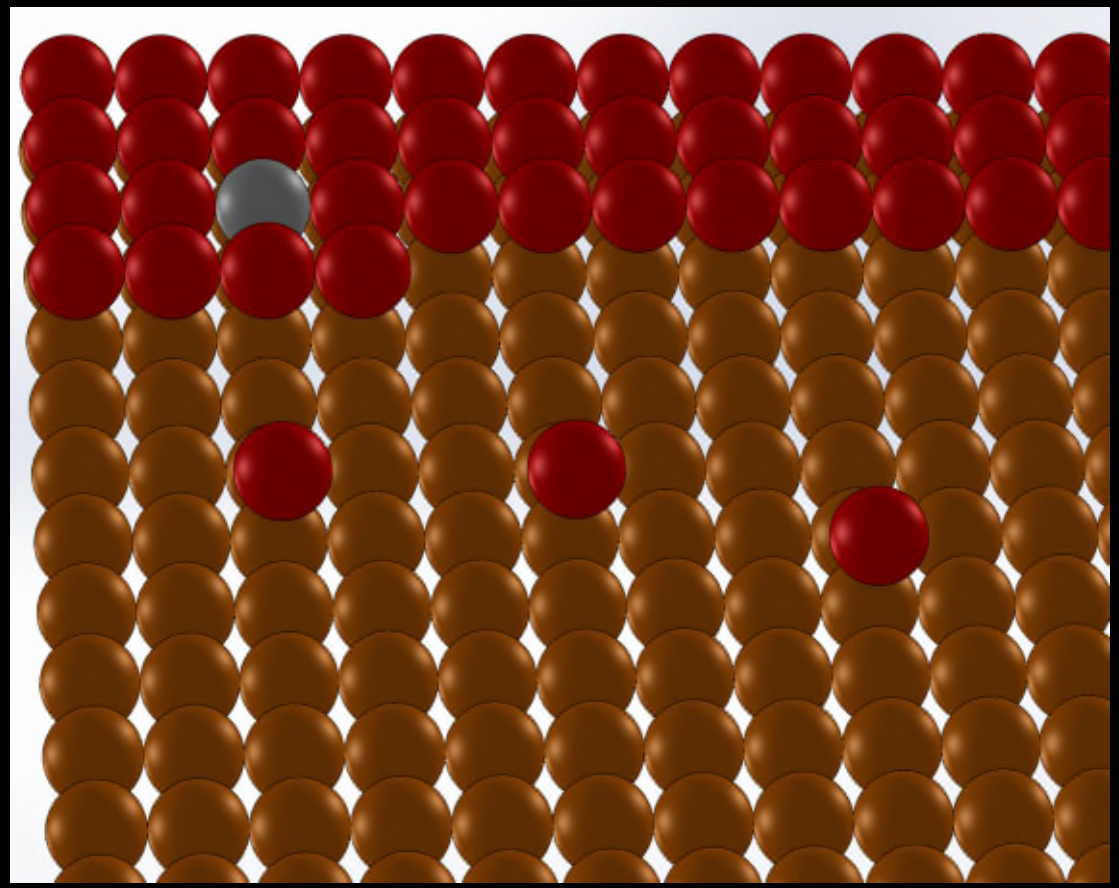






Solute trapping model for crystal growth

- Nanowire growth are modeled as a step growth process
- Solute trapping takes place when interface velocity approaches Ga diffusion rate

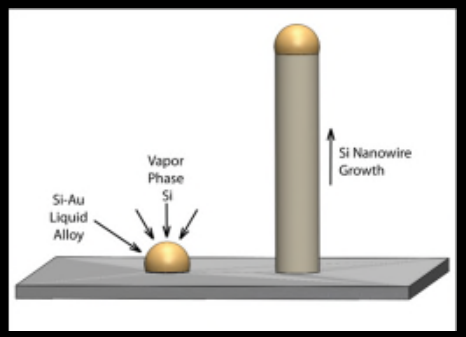


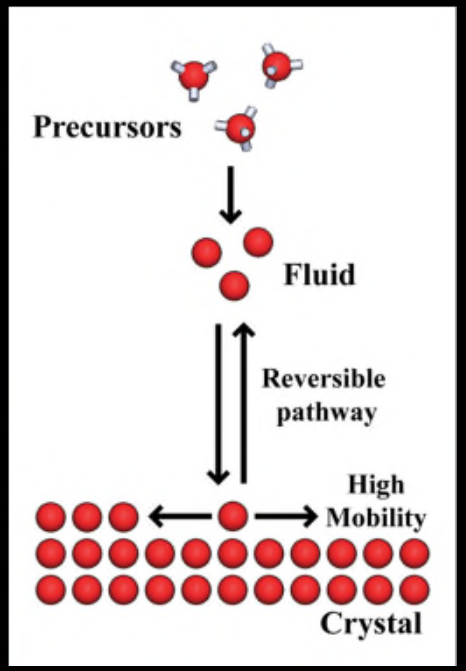
- Hypothesis:
- ***Higher temperatures*** allow Ga to have higher diffusivity, thus results in less Ga incorporation.
- ***Identity of liquid metal*** electrode will change the impurity incorporation rate.

Courtesy of Josh Demuth

Crystal Growth Conditions

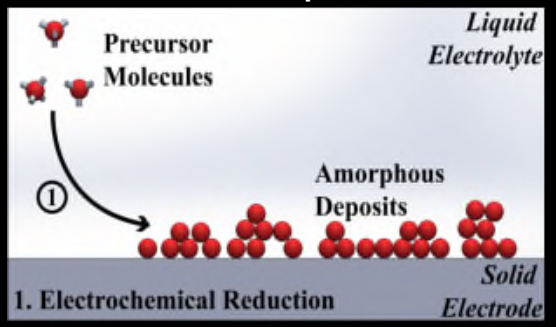
- VLS

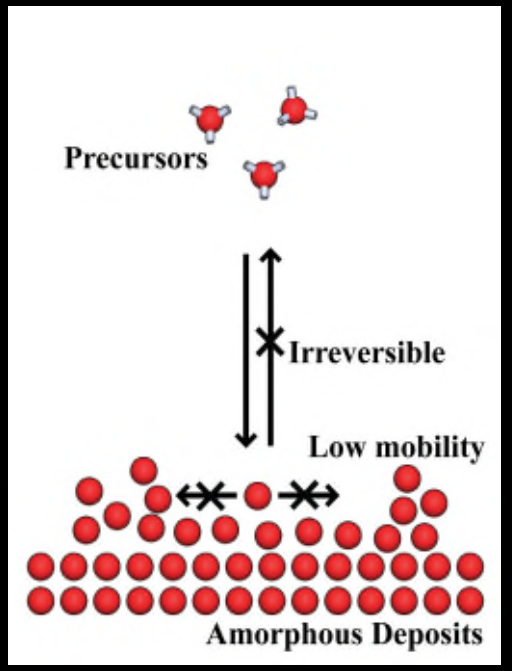




- High temperature
- Fluid phase

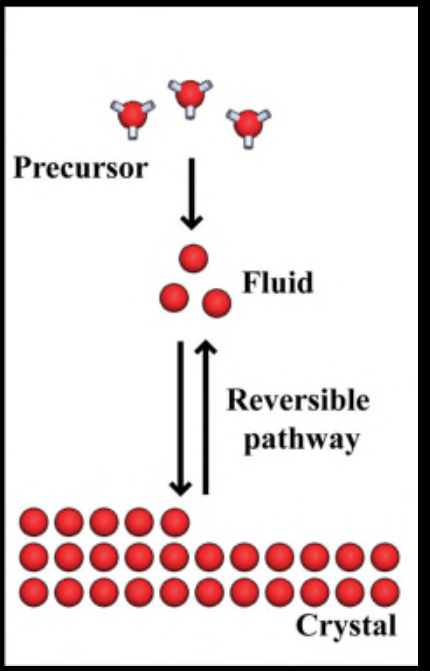
- Conventional electrodeposition





- Low temperature
- No fluid phase

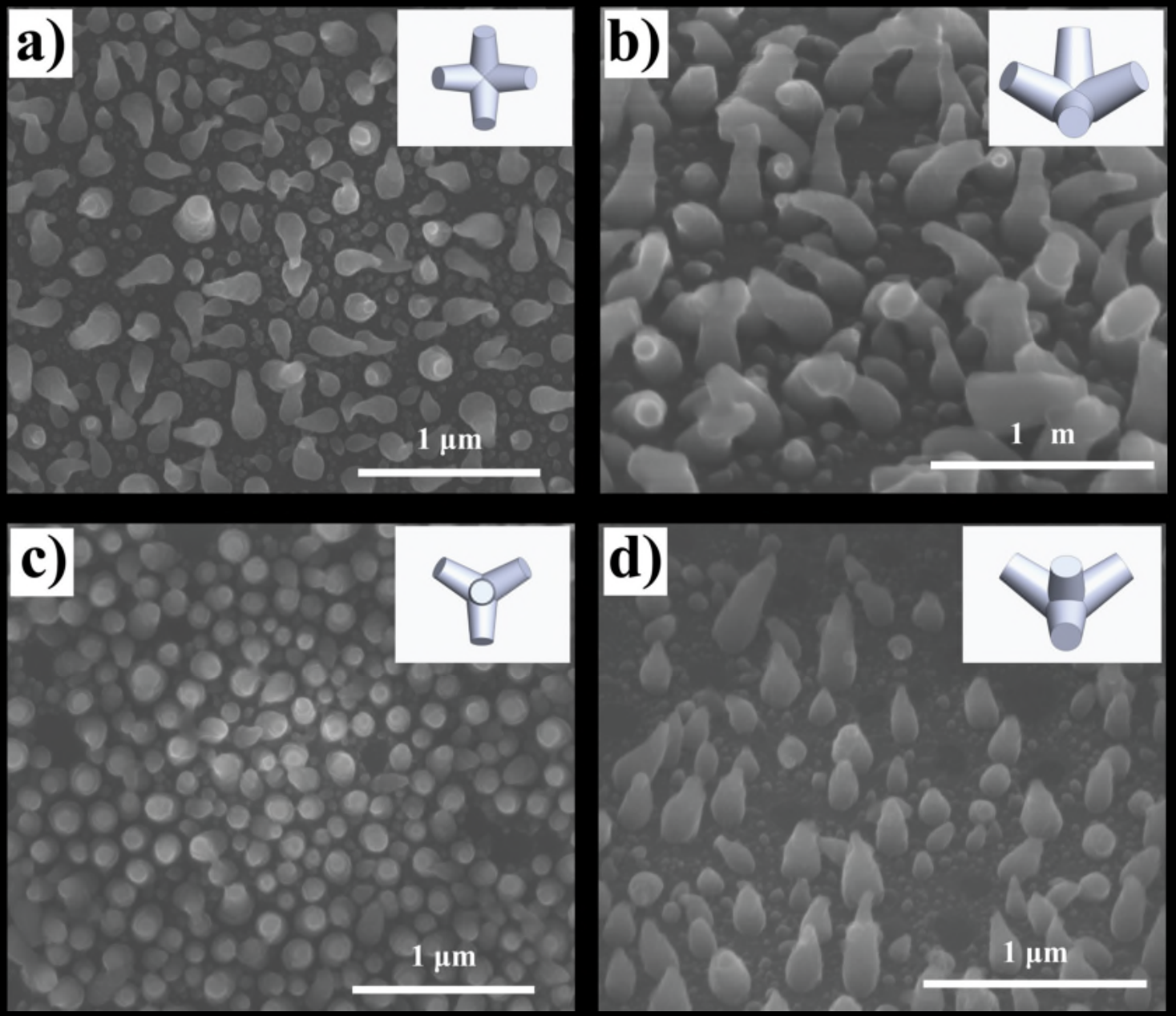
Unconventional electrodeposition



- Low temperature
- Fluid phase

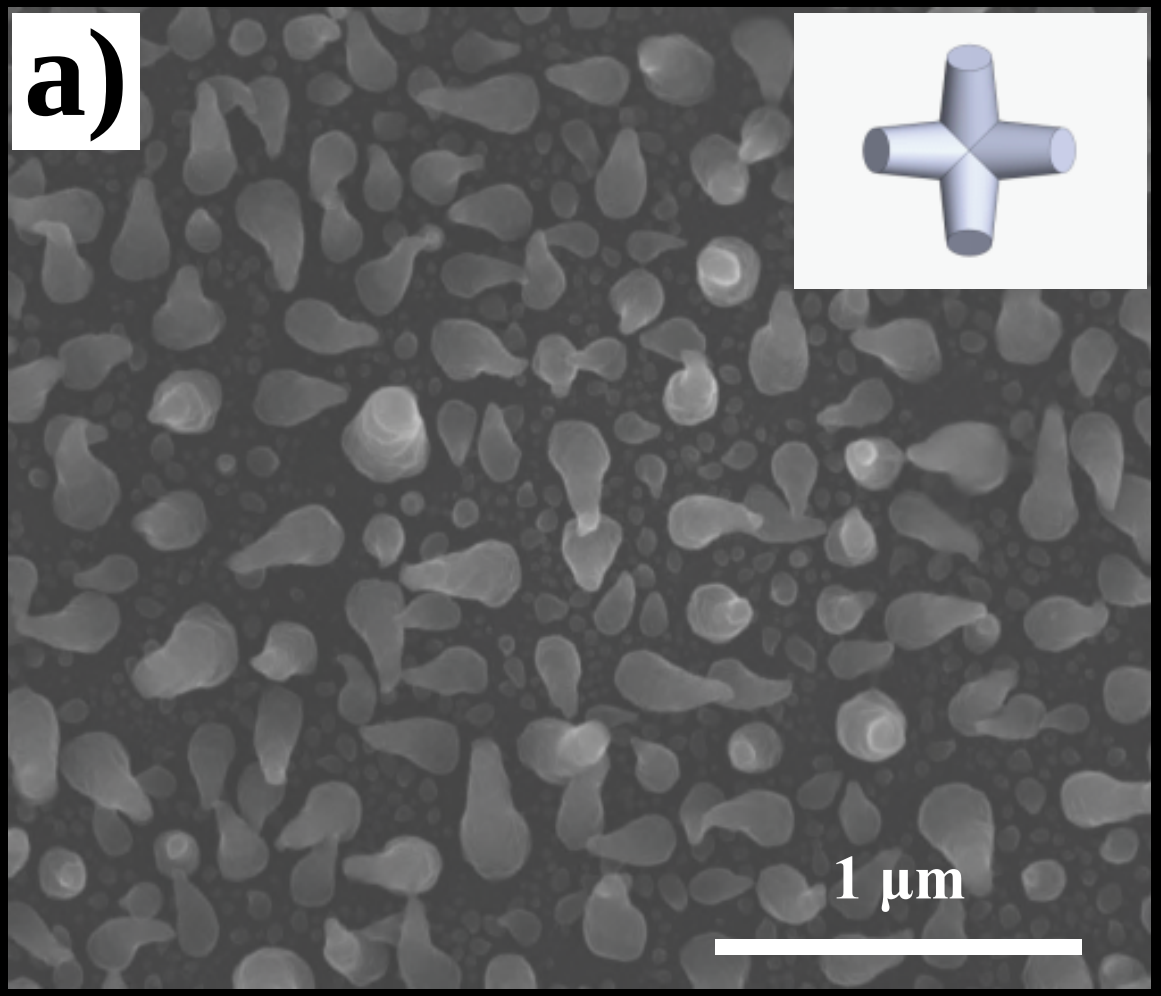
Vere, A. W. *Crystal growth: principles and progress*; Plenum Press: New York, 1987.

Scanning electron micrographs of SiNWs grown on Si(100) and Si(111) substrates

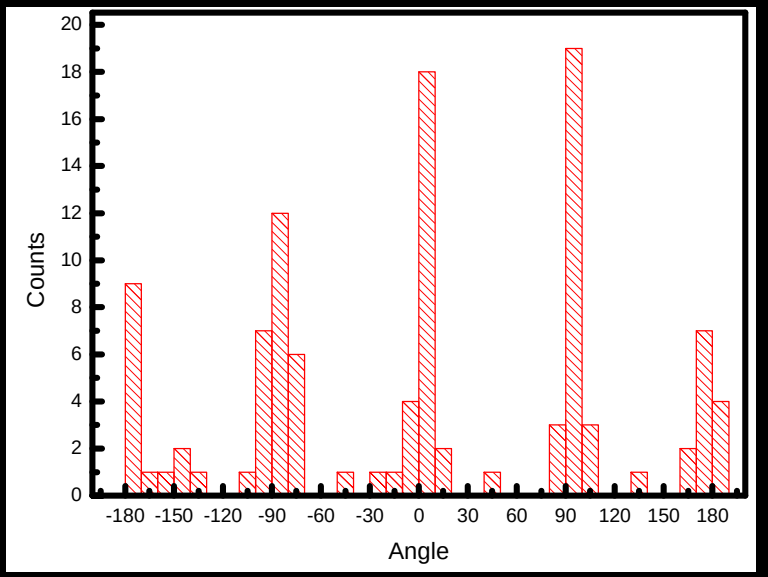


- Indirect evidence of epitaxy

Top-down view micrograph of SiNWs grown on Si(100)

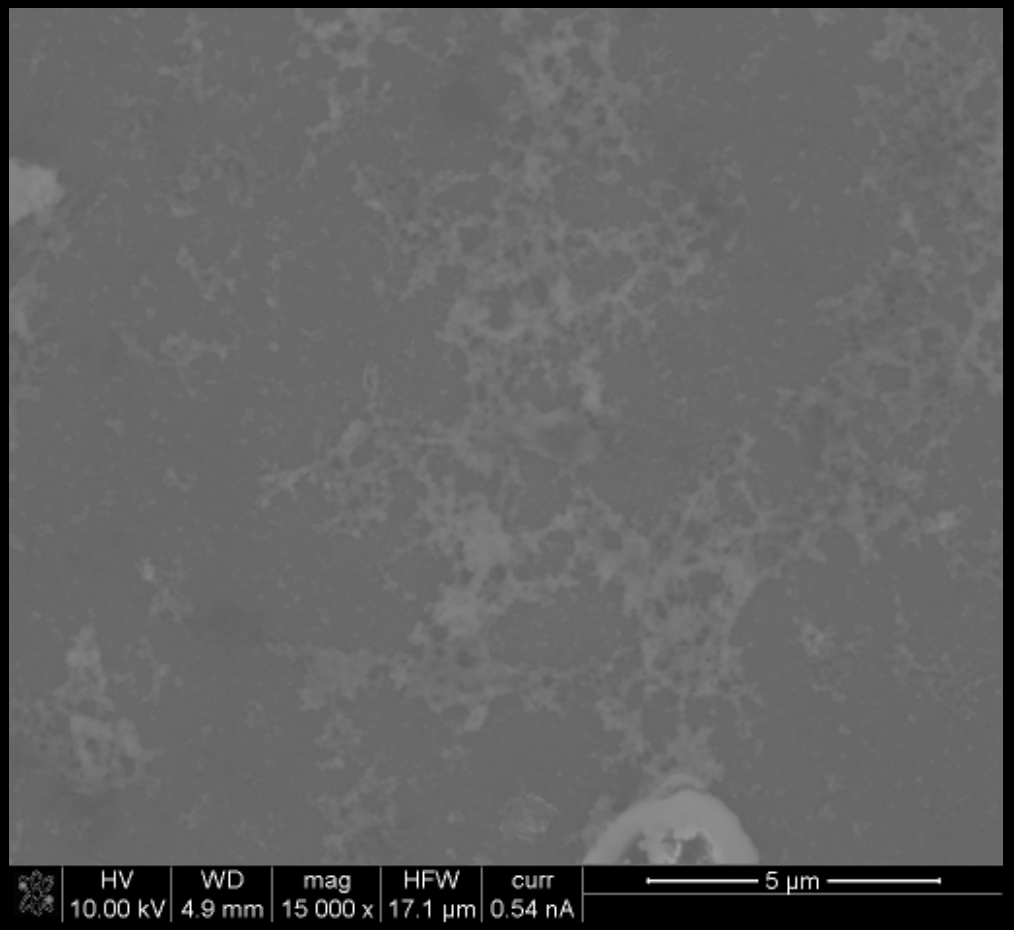


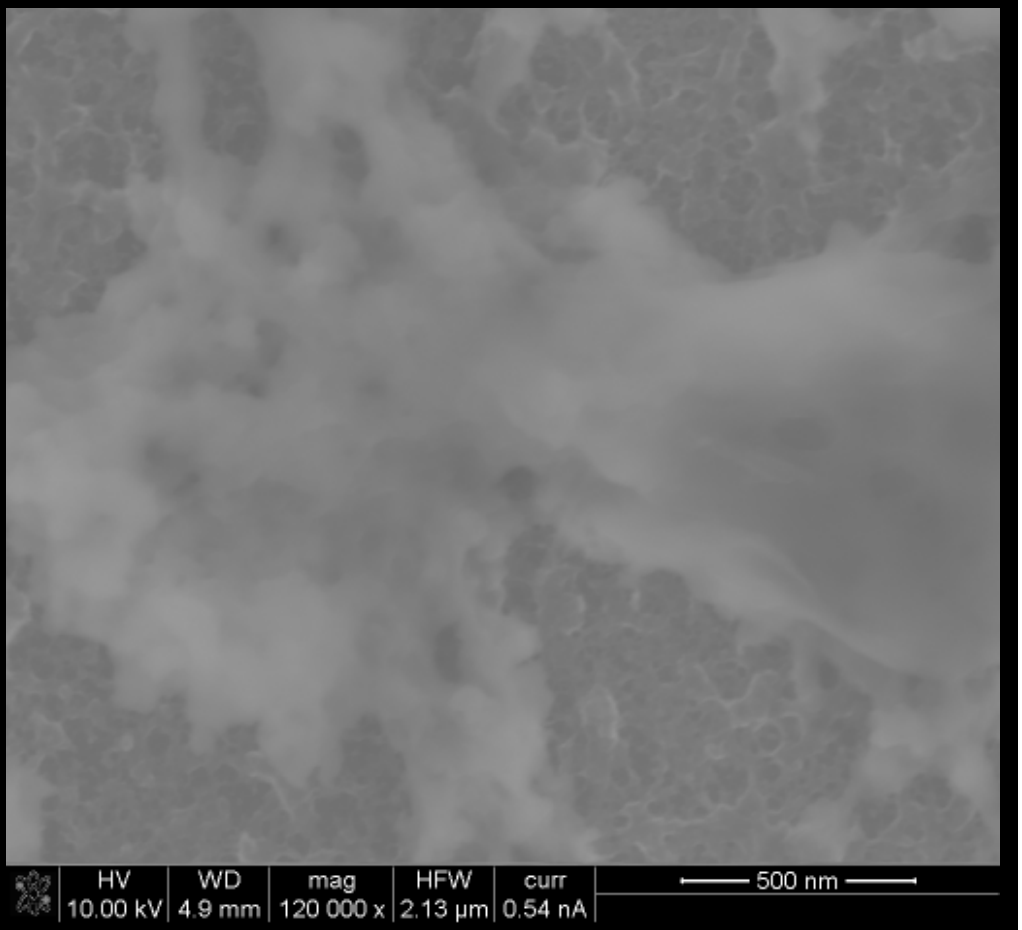
Given the growth orientation to be <111>, the nanowire grow continued at four distinct angles with 90° in-plane angle separation.



Using pure In to grow SiNWs

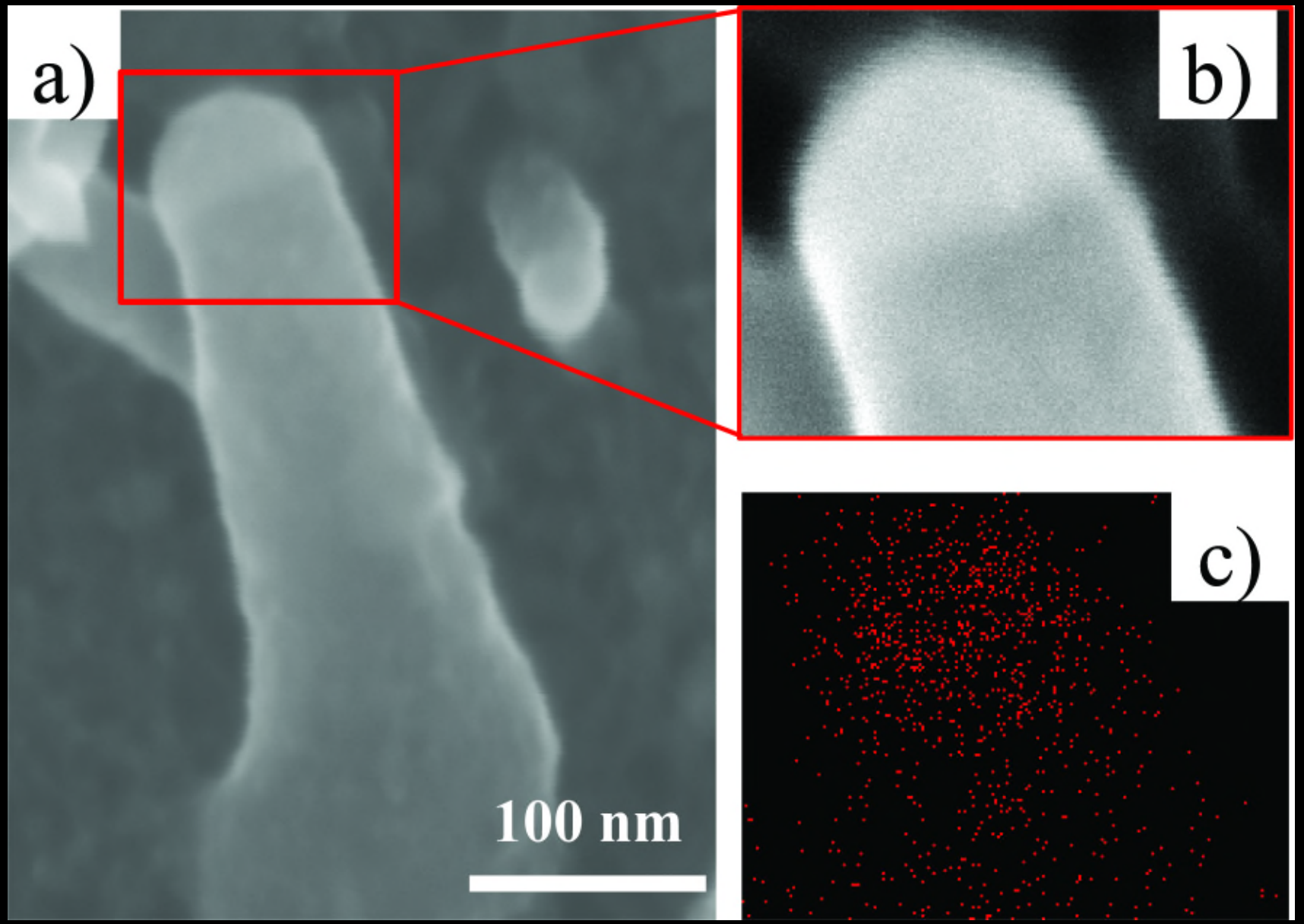
In: CA: -1.4 V, 300 s
Si: CA: 100 °C, -1.4 V, 1800s



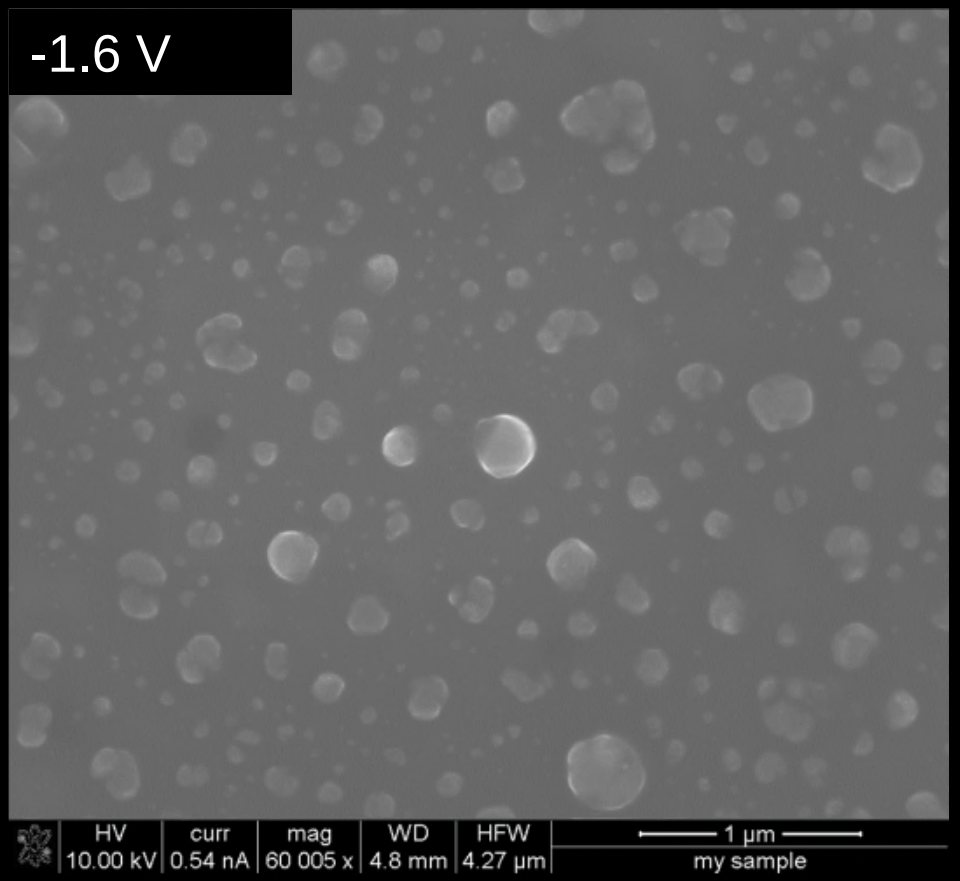


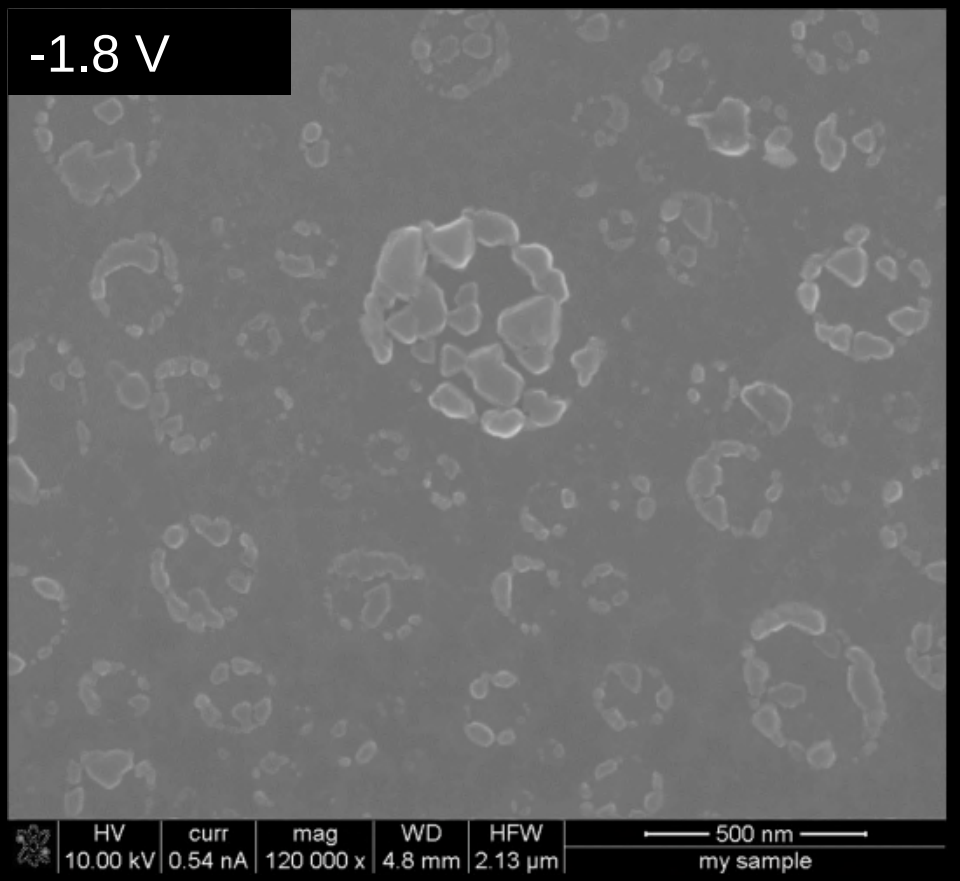
No Si deposit

Ga cap



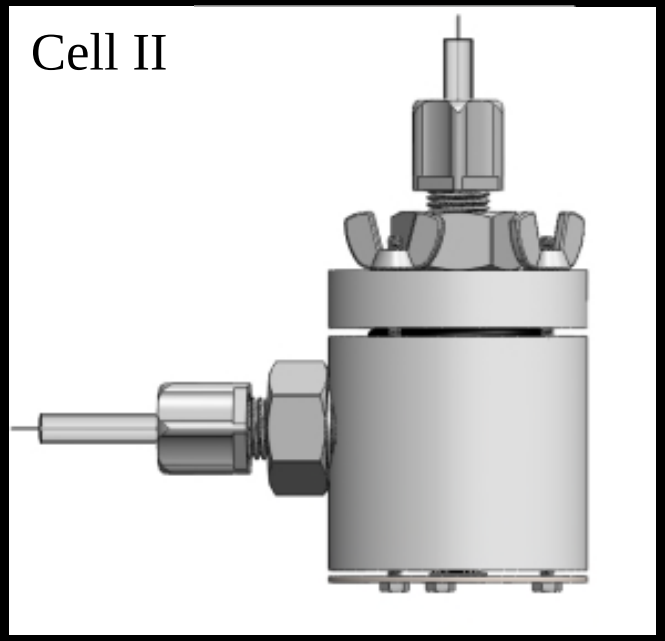
Try to deposit SiNWs at 200 °C



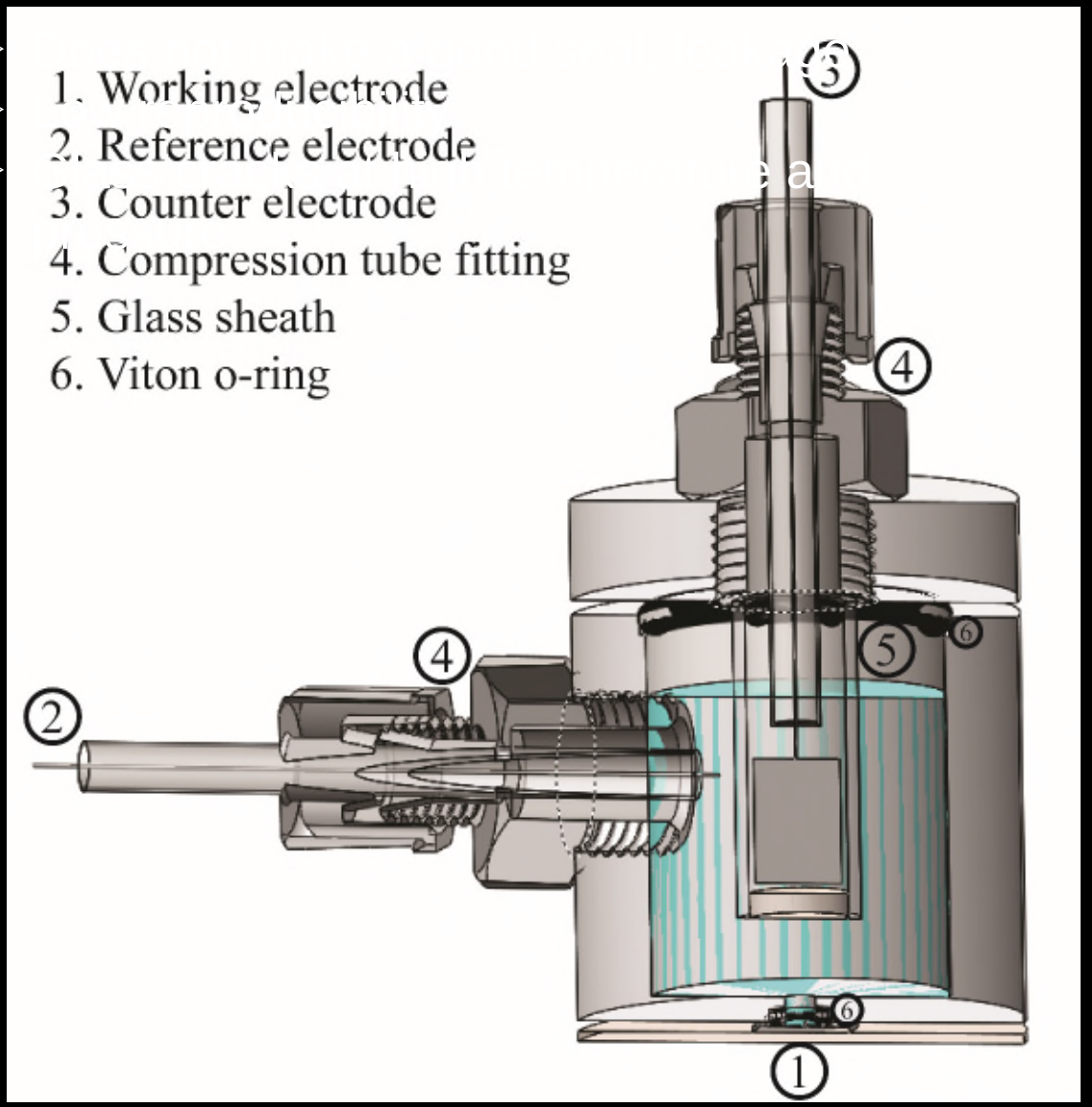


Ga etching were too fast at this temperature;
No Si deposit observed

New cell design – to accommodate high temperature experiments

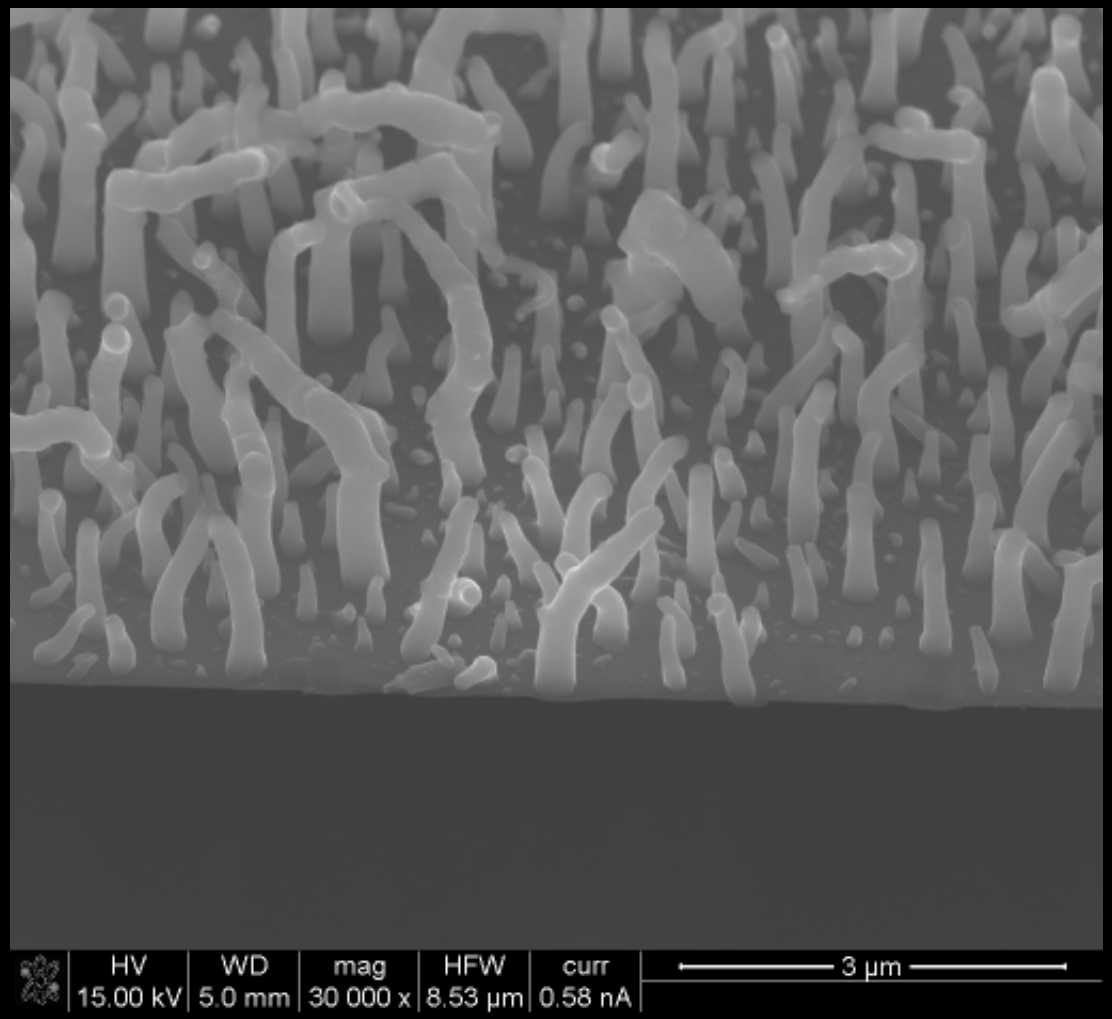


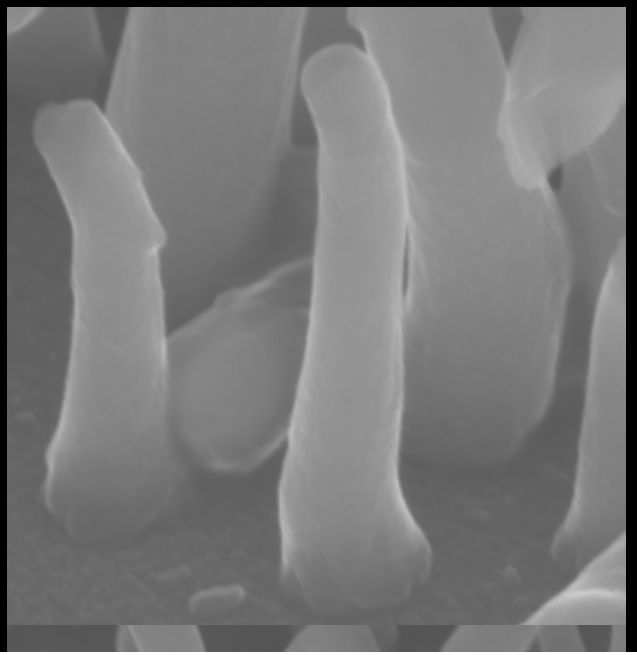
- Propylene carbonate boils at 242 °C
- $SiCl_4$ creates 400 psi gas vapor pressure at 200 °C
- Face type o-ring seals withstand up to 1000 psi
- Compression tube fittings withstand 50 ~ 220 psi at 20 °C;

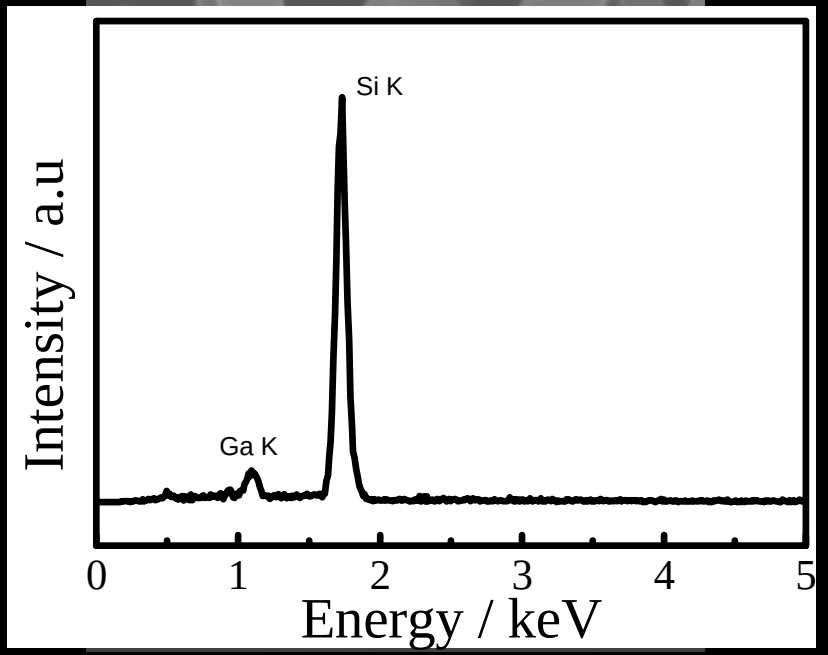


Potentiostatic deposition of SiNWs at 150 °C

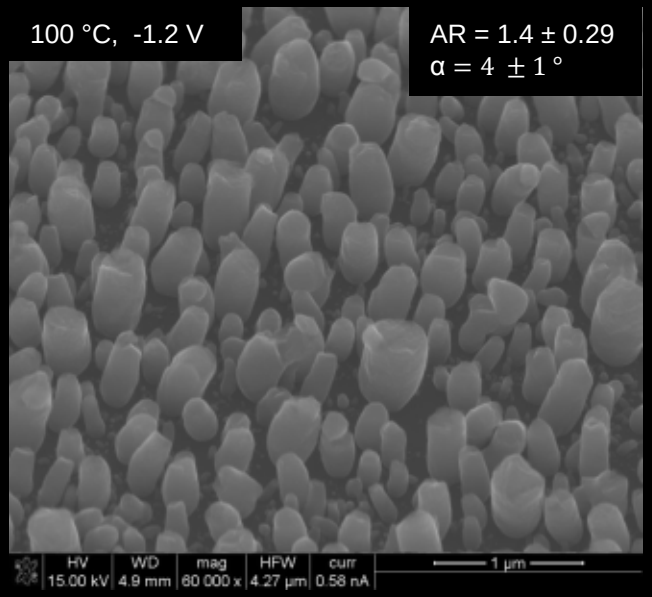
- -1.4 V vs Pt QRE, 30 mins

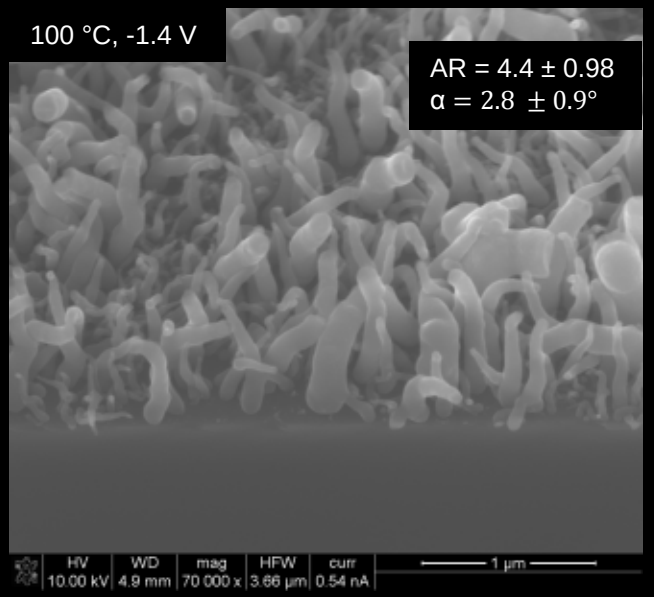


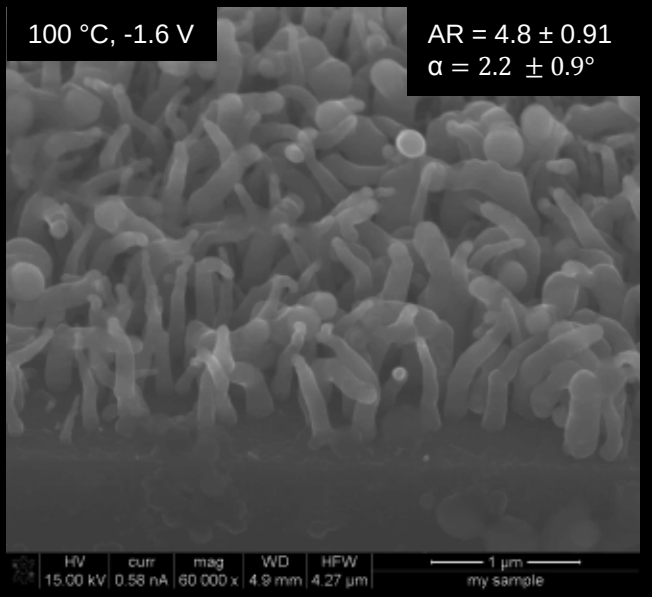
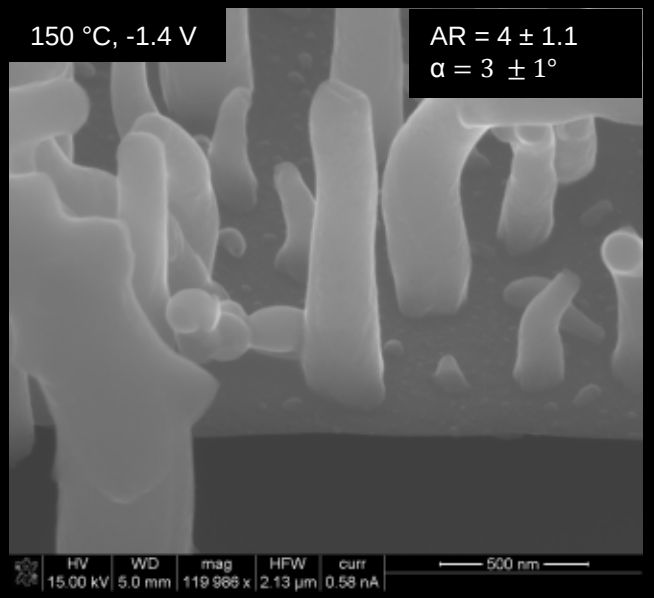
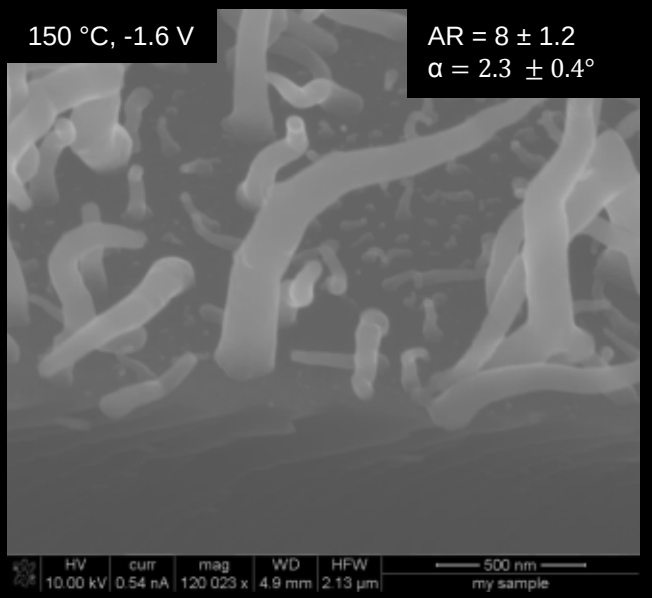




Nanowire length versus potential and temperature







- All deposition were 30 mins long
- ***Taper angle (α)*** at different temperatures and potentials are not significantly different
- Deposition potential affects nanowire ***aspect ratio (AS)***